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EXAMINER	
SAMUEL, DEWANDA A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,935	LEE, ROBERT J.	
	Examiner	Art Unit	
	DeWanda Samuel	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim1-20 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "a serial sync receiver that receives a serial packet sync datastream on a single" pin must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. **Claims 12,13, 19 and 20** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claims 12,13, 19 and 20, the limitation on a single pin needs to be further defined. Examine relied on the broadest interpretation. Appropriate correction required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. **Claims 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. (US Patent 6,973,096) in view of Mannette et al. (US Patent 6,975,652) and Feezel et al. (US Patent 5,267,263).

With regard to claim 1, Chappell et al. discloses a *method for supporting serial packet synchronization,* Chappell et al. discloses having a system and method for processing bandwidth allocation messages (Title).
in response to receiving a grant, latching a packet sync vector comprised of one or more bits into a serial packet sync transmitter; Chappell et al. discloses having a CM 106 (cable modem) shown in Fig. 2, the down stream physical communication circuit 124 may transmit a data stream 202 to the downstream MAC circuit (media access control) 128 in response to signals received from the CMTS 106 (Cable Modem Termination system) through the transmission medium 104... the data stream 202may comprise a series of MPEG data frames formatted according to International Telecommunication Recommendation "FIU-T J.83 where each MPEG data frame comprises a header 212 and payload 214. The payload 214 of one or more MPEG data frames may encapsulate a downstream DOCISIS MAC frame 204. A DODSIS MAC frame may have a payload comprising a MAC management message 205... the MAC management message 205 may comprise a MAC management header 210, a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-

bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218 ("in response receiving a grant", column 5 line 49-67)...forwarding the MAP Message payload 208 for processing as illustrated in fig. 4...a 32-bit shift register 304 ("transmitter") receives an 8-bit wide data stream from portions of a MAP management message ("latching a packet sync vector one or more bits into serial packet sync transmitter", column 6 line 39-54).

loading a preamble comprised of one or more bits into said serial packet sync transmitter, Chappell et al. discloses forwarding the MAP Message payload 208 for processing as illustrated in fig. 4.ooa 32-bit shift register 304 ("transmitter") receives an bit wide data stream from portions of a MAP management message ("latching a packet sync vector one or more bits into serial packet sync transmitter", column 6 line 39-54).

wherein said preamble and said packet sync vector form a serial packet sync data stream; Chappell et al. discloses the MAC management message 205 may comprise a MAC management header 210, a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218...(oolumn 5 line 62-67).

transmitting said serial packet sync data stream by synchronously, Chappell et al. discloses having a shared transmission medium may comprises an upstream passband in the transmission medium that is shared among the CM (cable modems) according a time division multiple access (TDMA) allocation scheme. It is known in the art that

TDMA is a type of time-division multiplexing and it has high synchronization overhead. So, it is inferred that transmitting of the data stream is synchronized.

shifting each bit of said serial packet sync datastream out of said serial packet sync transmitter; Chappell et al. discloses having 32-bit shift register receives 32-bit words in 8 bytes.., also, four 32-bit words of a MAP Message Header such as MAP Message Header 216 may be initially loaded in the Shifter register 304 before being forwarded to the data buffer 334. It is obvious that bits are being shifted in the shift register. However, Chappell does not explicitly discloses synchronously shifting each bit of said serial packet sync datastream out. Feezel et al. discloses having a synchronous transmitter for synchronously transmitting the second synchronous bit data stream (column 7 line 14-17).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a 32-bit shift register as taught by Chappell et al. synchronously transmitting the second synchronous bit data stream as taught by Feezel et al. to establish a bit by bit synchronization.

Chappell et al. does not disclose having *synchronously receiving each bit of said serial packet sync data stream into a serial packet sync receiver,*

Mannette et al. disclose having a CM (cable modem) that is responsible for receiving control message from the CMTS (). It is inferred that the CM receives synchronized message from the CMTS (cable modem termination system).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a cable modem 106 as taught by Chappell that receives synchronize message from the CMTS as taught by Mannette et al. to provide a more synchronized system; from the head end CMTS (cable modem termination system), to the CM (cable modem).

Chappell et al. does not disclose having *latching said packet sync vector into a holding register after comparing each bit of said serial packet sync data stream and determining that said serial packet sync data stream matches said preamble.* Mannette et al. discloses having the MPEG frame recover block 514 is coupled to MAC sync message detector 516. The MAC sync message detector 516 has a strobe, which coupled to timestamp registers 520, 522, 524, and 526, and the MAC sync message detector remote timestamp is coupled to registers 520. The registers 520 and 522 are coupled to modulo compare block 528 and register 520 coupled to register 522... (column 10 line 12-29)... timestamp registers 520,522,524, and 526 stores numerical values, which are representative of time. The values in these registers are latched by the strobe that comes from the MAC synchronous message detector 516... the modulo compare block 528 and 530 compares two different inputs and make a determination concerning the difference between the two inputs. The modulo compare block 530 determines the period of the local (CM) clock while the modulo compare block'528 determines the period of the remote clock (column 11 line 15-37). It is inferred that the MAC sync message is evaluated by the MAC message detector 516 and put into timestamp

registers ("holding registers") they are compared to the information that is given by the CMTS.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a cable modem 106 as taught by Chappell with timestamp registers 520, 522, 524, and 526 as taught by Mannette et al. to provide a mechanism that will accurately detect MAC sync messages that are in sync with the CMTS clock.

With regard to claim 3, in combination Chappell et al., Mannette et al. and Feezel et al. teaches the method recited in claim 1. *Further comprising the step of transmitting a non- unique bit sequence as said serial packet sync datastream.* Chappell et al. discloses having a system and method for processing bandwidth allocation messages (title). Chappell et al. further discloses having a message payload 208 may comprise a plurality of 32-bit words (column 5 line 62-67).

7. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. (US Patent 6,973,096) and Mannette et al (US Patent 6,975,652) and Feezel et al. (US Patent 5,267,263) as applied to claim 1 in further view of Moore, Jr. et al. (US Patent 6,807,195).

With regard to claim 2, in combination Chappell et al., Mannette et al. and Feezel et al. and teaches the method recited in claim 1. *Further comprising the step of generating an interrupt in response to executing said latching step.* Chappell et al.

discloses having a system and method for processing bandwidth allocation messages. However, Chappell et al. does not disclose generating an interrupt in response to executing said latching step. Moore Jr. et al. discloses having synchronization arrangement for packet cable telephony modem (title). Moore Jr, et al. further discloses having a host interface 66 interrupted by DSP 60 (digital signal processor) every time a packet is assembled and ready for transmission (column 4 line 21-23).
Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have having a system and method for processing bandwidth allocation messages as taught by Chappell et al. with a synchronization arrangement for packet cable telephony modem (Title) whereby controlling the timing of the creation and transmission of upstream voice packets with respect to received upstream grant as taught by Moore Jr, et al. to minimize the inherent packet characteristics of latency.

With regard to claim 4, in combination Chappell et al., Mannette et al. and Feezel et al. and teaches the method recited in claim 1. *Wherein said transmitting step further comprises the step of synchronizing the transmitting of said serial packet sync datastream to a VoIP clock signal.* Chappell et al. discloses having a system and method for processing bandwidth allocation messages. However, Chappell et al. does not explicitly disclose comprises the step of synchronizing the transmitting of said serial packet sync datastream to a VoIP clock signal. Moore Jr, et al. discloses having a bi-directional cable system with a synchronization arrangement for packet cable telephony

modem...also to improve the upstream transmission of packet voice data through an HFC network and to include a synchronization unit in the subscriber broadband terminal interface unit to control the timing of the creation and transmission of upstream voice packets with respect to received upstream grant (Title and column 2 line 16-67). Moore Jr, et al further discloses in fig. 4 a programmable logic device (PLD) 72 is used to implement the synchronization process...also a phase-lock loop (PLL) 74 is used to provide a basic clock signal CK to PLD 72, where the CK signal is derived from timing within the CMTS (not shown, column 4 line 46-67). It is inferred that the transmission of packet voice traffic are in sy.nc with the CMTS.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have having a system and method for processing bandwidth allocation messages as taught by Chappell et al. with a synchronization arrangement for packet cable telephony modem (Title) whereby controlling the timing of the creation and transmission of upstream voice packets with respect to received upstream grant as taught by Moore Jr, et al. to minimize the inherent packet characteristics of latency and jitter.

8. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. (US Patent 6,973,096) and Mannette et al (US Patent 6,975,652) and Feezel et al. (US Patent 5,267,263) as applied to claim 1 in further view of Chapman (US Patent 7,085,287).

With regard to claim 5, in combination Chappell et al., Mannette et al. and Feezel et al. teaches the method recited in claim 1. *Further comprising the step of preselecfing a unique bit sequence as said preamble.* Chappell et al. discloses having a system and method for processing bandwidth allocation messages. However, Chappell et al. does not explicitly disclose having the step of preselecting a unique bit sequence as said preamble. Chapman discloses assigning a unique SID (service identification, "preamble", column 13 line 41- 42)...also the SID address per upstream channel, each node (e.g. cable4 modem) in the HFC network has associated with it a unique SID value which may be independent from the domain in which that the cable modem is a member (column 11 line 60-67).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have having a system and method for processing bandwidth allocation messages as taught by Chappell et al. with a addressing scheme that assigns SID (service identification, "preamble") a unique value as taught by Chapman to prevent overlap between different DOCSIS domains and allow extreme flexibility domain assignments within the CMTS, which is logically based.

9. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. (US Patent 6,973,096) in view of Feezel et al. (US Patent 5,267,263).

With regard to claim 6, Chappell et al. discloses a *method for supporting serial packet synchronization,* Chappell et al. discloses having a system and method for processing bandwidth allocation messages.

in response to receiving a grant, latching a packet sync vector comprised of one or more bits into a serial packet sync transmitter; Chappell et al. discloses having a CM 106 (cable modem) shown in Fig. 2, the down stream physical communication circuit 124 may transmit a data stream 202 to the downstream MAC circuit (media access control) 128 in response to signals received from the CMTS 106 (Cable Modem Termination system) through the transmission medium 104... the data stream 202may comprise a series of MPEG data frames formatted according to International Telecommunication Recommendation FIU-T J.83 where each MPEG data frame comprises a header 212 and payload 214. The payload 214 of one or more MPEG data frames may encapsulate a downstream DOCISIS MAC frame 204. A DODSIS MAC frame may have a payload comprising a MAC management message 205... the MAC management message 205 may comprise a MAC management header 210, a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218 ("in response receiving a grant", column 5 line 49-67)...forwarding the MAP Message payload 208 for processing as illustrated in fig. 4...a 32-bit shift register 304 ("transmitter") receives an 8-bit wide data stream from portions of a MAP management message ("latching a packet sync vector one or more bits into serial packet sync transmitter", column 6 line 39-54).

loading a preamble comprised of one or more bits into said serial packet sync transmitter, Chappell et al. discloses forwarding the MAP Message payload 208.for processing as illustrated in fig. 4...a 32-bit shift register 304 :("transmitter") receives an bit wide data stream from portions of a MAP management message ("latching a packet sync vector one or more bits into serial packet sync transmitter", column 6 fine 39-54).

wherein said preamble and said packet sync vector form a serial packet sync datastream; Chappell et al. discloses the MAC management message 205 may comprise a MAC management header 210, a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218...(column 5 line 62-67).

transmitting said serial packet sync datastream by synchronously shifting each bit of said serial packet sync datastream out of said serial packet sync transmitter. Chappell et al. discloses having 32-bit shift register receives 32-bit words in 8 bytes.., also, four 32-bit words of a MAP Message Header such as MAP Message Header 216 may be initially loaded in the shifter register 304 before being forwarded to the data buffer 334. It is obvious that bits are being shifted in the shift register. However, Chappell does not explicitly discloses synchronously shifting each bit of said serial packet sync datastream out. Feezel et al. discloses having a synchronous transmitter for synchronously transmitting the second synchronous bit data stream (column 7 line 14-17).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a 32-bit shift register as taught by Chappell et al. synchronously transmitting the second synchronous bit data stream as taught by Feezel et al. to establish a bit by bit synchronization.

With regard to claim 7, in combination Chappell et al. and Feezel et al. teaches the method recited in claim 6. *Further comprising the step of transmitting a non-unique bit sequence as said serial packet sync datastream;* Chappell et al. discloses having a system and method for processing bandwidth allocation messages. Chappell et al. further discloses having a message payload 208 may comprise a plurality of 32-bit words (column 5 line 62-67).

10. Claim 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. (US Patent 6,973,096) and Feezel et al. (US Patent 5,267,263) as applied to claim 6 in further view of Chapman (US Patent 7,085,287).

With regard to claim 8, in combination Chappell et al. and Feezel et al. teaches the method recited in claim 6. Wherein said transmitting step further comprises the step of synchronizing the transmitting of said serial packet sync datastream to a VoIP clock signal.

Chappell et al. discloses having a system and method for processing bandwidth allocation messages. However, Chappell et al. does not explicitly disclose comprises

the step of synchronizing the transmitting of said serial packet sync datastream to a VoIP clock signal. Moore Jr, et al. discloses having a bi-directional cable system with a synchronization arrangement for packet cable telephony modem...also to improve the upstream transmission of packet voice data through an HFC networkand to include a synchronization unit in the subscriber broadband terminal interface unit to control the timing of the creation and transmission of upstream voice packets with respect to received upstream grant (Title and column 2. line 16-67). Moore Jr, et al further discloses in fig. 4 a programmable logic device (PLD) 72 is used to implement the synchronization process...also a phase-lock loop (PLL) 74 is used to provide a basic clock signal CK to PLD 72, where the CK signal is derived from timing within the CMTS (not shown, column 4 line 46-67). It is inferred that the transmission of packet voice traffic are in sync with the CMTS.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have having a system and method for processing bandwidth allocation messages as taught by Chappell et al. with a synchronization arrangement for packet cable telephony modem (Title) whereby controlling the timing of the creation and transmission of upstream voice packets with respect to received upstream grant as taught by Moore Jr, et al. to minimize the inherent packet characteristics of latency and jitter.

With regard to claim 9, in combination Chappell et al. and Feezel et al. teaches the method recited in claim 6.Further comprising the step of preselecting a unique bit

sequence as said preamble. Chappell et al. discloses having a system and method for processing bandwidth allocation messages. However, Chappell et al. does not explicitly disclose

having the step of preselecting a unique bit sequence as said preamble. Chapman discloses assigning a unique SID (service identification, "preamble", column 13 line 41-42)...also the SID address per upstream channel, each node (e.g. cable4 modem) in the HFC network has associated with it a unique SID value which may be independent from the domain in which that the cable modem is a member (column 11 line 60-67).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have having a system and method for processing bandwidth allocation messages as taught by Chappell et al. with a addressing scheme that assigns SID (service identification, "preamble") a unique value as taught by Chapman to prevent overlap between different DOCSIS domains and allow extreme flexibility domain assignments within the CMTS, which is logically based.

11. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. (US Patent 6,973,096) in view of Gatherer et al. (US Patent 6,549,584) and Mannett et al. (US Patent 6,975,652).

With regard to claim 10, Chappell et al. discloses a method for supporting serial packet synchronization, Chappell et al. discloses having a system and method for processing bandwidth allocation messages.

Chappell et al. does not disclose synchronously receiving each bit of a serial packet sync datastream into a serial packet sync receiver, Gatherer et al. discloses having a receiving side ("receiver") of the cable modem 10 thereby receiving downstream signal ("serial packet sync datastream") from the central office modem 12 (column 13 line 15-25). It is inferred that the cable modem 10 must be sync with the central office modem 12 in order to transmit data during the allocated time slot.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a cable modem 106 as taught by Chappell with a receiving side ("receiver") that receives downstream signal ("serial packet sync datastream") from the central office modem 12 as taught by Gatherer et al. provide synchronization within the system.

wherein said serial packet sync datastream is comprised of a packet sync vector and a preamble; Chappell et al. discloses the MAC management message 205 may comprise a MAC management header 210 ("preamble"), a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218...(column 5 line 62-67).

Chappell et al. does not disclose having latching said packet sync vector into a holding

register after comparing each bit of said serial packet sync data stream and determining that said serial packet sync data stream matches said preamble. Mannette et al. discloses having the MPEG frame recover Block 514 is coupled to MAC sync message detector 516. The MAC sync message detector 516 has a strobe, which coupled to timestamp registers 520, 522, 524, and 526, and the MAC sync message detector remote timestamp is coupled to registers 520. The registers 520 and 522 are coupled to modulo compare block 528 and register 520 coupled to register 522... (column 10 line 12-29)...timestamp registers 520,522,524, and 526 stores numerical values, which are representative of time. The values in these registers are latched by the strobe that comes from the MAC synchronous message detector 516... the modulo compare block 528 and 530 compares two different inputs and make a determination concerning the difference between the two inputs. The modulo compare block 530 determines the period of the local (CM) clock while the modulo compare block 528 determines the period of the remote clock (column 11 line 15-37). It is inferred that the MAC sync message is evaluated by the MAC message detector 516 and put into timestamp registers ("holding registers") they are compared to the information that is given by the CMTS.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a cable modem 106 as taught by Chappell with timestamp registers 520, 522, 524, and 526 as taught by Mannette et al. to provide a mechanism that will accurately detect MAC sync messages that are in sync with the

CMTS clock.

12. **Claim 11** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chappell et al. (US Patent 6,973,096) Gatherer et al. (US Patent 6,549,584) and Mannett et al. (US Patent 6,975,652) as applied to claim 10 in further view of Moore, Jr. et al. (US Patent 6,807,195)

With regard to claim 11, in combination Chappell teaches the method recited in claim 10. Further comprising the step of generating an interrupt in response to said latching step. Chappell et al. discloses having a system and method for processing bandwidth allocation messages. However, Chappell et al. does not disclose generating an interrupt in response to executing said latching step. Moore Jr. et al. discloses having synchronization arrangement for packet cable telephony modem (title). Moore Jr, et al. further discloses having a host interface 66 interrupted by DSP 60 (digital signal processor) every time a packet is assembled and ready for transmission (column 4 line 21-23).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have having a system and method for processing bandwidth allocation messages as taught by Chappell et al. with a synchronization arrangement for packet cable telephony modem (Title) whereby controlling the timing of the creation and transmission of upstream voice packets with respect to received

upstream grant as taught by Moore Jr, et al. to minimize the inherent packet characteristics of latency.

13. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gatherer et al. (US Patent 6,549,584) as applied to claim 12 above, and further in view of Krieger (US Patent 6,769,093).

With regard to claim 13, Gatherer et al. teaches the system recited in claim 12. Wherein said serial packet sync encoder comprises a serial packet sync transmitter that transmits said serial packet sync datastream on a single pin. Gatherer et al. discloses having a system topology of a cable television network (CATV, column 6 line 46-48). Gatherer et al. further discloses having an Encoder 28 in fig. 8 that receives bitstream B from MAC and interface function 26... (column 8 66-67). However, Gatherer et al. does not explicitly discloses having serial packet sync encoder comprises a serial packet sync transmitter that transmits said serial packet sync datastream on a single pin.. Krieger disclose having a encoder 116 at the transmitter is a SCTCM encoder (serially concatenated trellis coded modulation, column 5 line 41-42).It is inferred the SCTCM encoder serially process data.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a encoder 28 as taught by Gatherer et al. that is a SCTCM encoder (serially concatenated trellis coded modulation, column 5 line 41- 42)

that comprises a transmitter as taught by Krieger to provide a technique that will encode each bit in order to detect errors within the data words that are transmitted.

14. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gatherer et al. as applied to claim 12 above, and further in view of Mannette et al. (US Patent 6,975,652).

With regard to claim 14, Gatherer et al. teaches the system recited in claim 12. Wherein said serial packet sync receiver; Gatherer et al. discloses having a system topology of a cable television network (CATV, column 6 line 46-48) and cable modem 10 with a receiving side. It is obvious that the cable modem includes a receiver.
a preamble comparator that compares said received serial packet sync datastream to determine if said received serial packet sync datastream matches a preamble; a holding register for holding said packet sync vector.
Mannette et al. discloses having the MPEG frame recover block 514 is coupled to MAC sync message detector 516. The MAC sync message detector 516 has a strobe ("preamble comparator"), which coupled to timestamp registers 520, 522, 524, and 526 ("holding registers"), and the MAC sync message detector remote timestamp is coupled to registers 520. The registers 520 and 522 are coupled to modulo compare block 528 and register 520 coupled to register 522... (column 10 line 12-29)... timestamp registers 520,522,524, and 526 stores numerical values, which are representative of time. The values in these registers are latched by the strobe that comes from the MAC

synchronous message detector.516.., the modulo compare block 528 and 530 compares two different inputs and make a determination concerning the difference between the two inputs. The modulo compare block 530 determines the period of the local (CM) clock while the modulo compare block 528 determines the period of the remote clock (column 11 line 15-37). It is inferred that the MAC sync message is evaluated by the MAC message detector 516 and put into timestamp registers ("holding registers") they are compared to the information that is given by the CMTS.

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a cable modem 10 with a receiving side as taught by Gatherer et al. with a MAC sync message detector 516 with a strobe ("preamble comparator") and timestamp registers 520, 522, 524, and 526 as taught by Mannette et al. to provide a mechanism that will accurately detect MAC sync messages that are in sync with the CMTS clock.

15. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gatherer et al. (US Patent 6,549,584) as applied to claim 12 above, and further in view of Coles et al. (PG PUB 2004/0150537 A1).

With regard to claim 15, Gatherer et al. teaches the system recited in claim 12. Wherein said serial packet sync transmitter and said serial packet sync receiver are shift registers. Gatherer et al. discloses having a system topology of a cable television

network (CATV, column 6 line 46-48) with a coding scheme in a cable modem (title). However, Gatherer et al does not discloses having a said serial packet sync transmitter and said serial packet sync receiver are shift registers. Coles discloses having transmitting of data words and code word synchronization... (abstract). Coles further discloses having a shift registers in the transmitter and receiver... (page 3 paragraph 38 line 1-2).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a cable modem as taught by Gatherer et al. with a scheme to synchronize code words further utilizing shift registers in the transmitter and receiver as taught by Coles et al. to maintain synchronization within the system.

16. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gatherer et al. as applied to claim 12 above, and further in view of Chappell (US Patent 6,973,096).

With regard to claim 16, Gatherer et al. teaches the system recited in claim 12. Wherein said serial packet sync datastream is comprised of a non-unique bit sequence. Gatherer et al. discloses having a system topology of a cable television network (CATV, column 6 line 46-48) with a coding scheme for cable modems (title) However, Gatherer et al. does not explicitly disclose said serial packet sync datastream is comprised of a

non-unique bit sequence. Chappell et al. discloses having a system and method for processing bandwidth allocation messages. Chappell et al. further discloses having a message payload 208 may comprise a plurality of 32-bit words (column 5 line 62-67). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a system topology of a cable television network (CATV, column 6 line 46-48) with a coding scheme for cable modems (title) as taught by Gatherer et al. with a message payload 208 with a plurality of 32-bit words as taught by Chappell et al. to provide a numbering scheme that is recognizable in the system.

With regard to claim 17, Gatherer et al. teaches the system recited in claim 12. Wherein after receiving a grant, said serial packet sync datastream is comprised of said packet sync vector and said preamble. Gatherer et al. discloses having a system topology of a cable television network (CATV, column 6 line 46-48) with a coding scheme for cable modems (title). However, Gatherer et al. does not explicitly disclose wherein after receiving a grant, said serial packet sync datastream is comprised of said packet sync vector and said preamble. Chappell et al. discloses the MAC management message 205 may comprise a MAC management header 210 ("preamble"), a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218...(column 5 line 62-67)...also, the MAC management

message 205 includes a SID (service identifier, "packet sync vector", column 6 line 11-13)

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a system topology of a cable television network (CATV, column 6 line 46-48) with a coding scheme for cable modems (title) as taught by Gatherer et al. with a MAC management message 205 may comprise a MAC. management header 210 ("preamble") and a SID (service identifier, "packet sync vector") as taught by Chappell et al. to advantageously provide a message format that will define the type of data that is being transmitted.

With regard to claim 18, in combination Gatherer et al. and Chappell et al. teaches the system recited in claim 12. Wherein said preamble is a preselected unique bit sequence. Gatherer et al. discloses having a system topology of a Cable television network (CATV, column 6 line 46-48) with a coding scheme for cable modems (title). However, Gatherer et al. does not explicitly disclose said preamble is a preselected unique bit sequence. Chapman discloses assigning a unique SID (service identification, "preamble", column 13 line 41-42)...also the SID address per upstream channel, each node (e.g. cable4 modem) in the HFC network has associated with it a unique SID value which may be independent from the domain in which that the cable modem is a member (column 11 line 60-67).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a system topology of a cable television network (CATV, Column 6 line 46-48) with a coding scheme for cable modems (title) as taught by Gatherer et al. with a unique SID (service identification, "preamble") as taught by Chappell et al. to uniquely define the CM (cable modem) that request for a allocated time slot.

17. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gatherer et al. (US Patent 6,549,584) in view of Chappell et al. (US Patent 6,973,096) and Krieger (US Patent 6,796,093).

With regard to claim 19, Gatherer et al. discloses a system for transmitting indication of an event, comprising: a media access controller that asserts a packet sync vector in response to receiving a grant; Gatherer et al. discloses having a cable modem 10 with a media access control (MAC) mechanism...the MAC operation particularly in allocating upstream communication slots and managing upstream timing (column 7 line 33-48). The MAC (media access control) has the capability to create a packet sync vector in response to receiving its allocated bandwidth within a time slot.
a serial packet sync encoder that encodes a serial packet sync datastream, (column 8 66-67); Gatherer et al. disclose having a Encoder 28 in fig. 8 that receives bitstream B from MAC and interface function 26... (column 8 66-67).

Gatherer does not disclose said serial packet sync datastream comprised of said packet sync vector and a preamble, Chappell et al. discloses the MAC management message 205 may comprise a MAC management header 210 ("preamble"), a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218...(column 5 line 62-67).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a cable modem 10 with a media access control (MAC) mechanism as taught by Gatherer et al. MAC management message 205 may comprise a MAC management header 210 ("preamble"), a message payload 218, and CRC 206...the message payload 208 may comprise a plurality of 32-bit words. These 32-bit word may comprise bandwidth allocation elements (MAPS) such as data grant MAP elements 218...(column 5 line 62-67) as taught by Chappell et al. to provide a technique for transmitting a data that describes the transmission and what type of data is in the message.

wherein said serial packet sync encoder comprises a serial packet sync transmitter that transmits said serial packet sync datastream on a single pin as an indication that said grant has arrived. Gatherer et al. discloses having a system topology of a cable television network (CATV, column 6 line 46-48). Gatherer et al. further discloses having an Encoder 28 in fig. 8 that receives bitstream B from MAC and interface function

26... (column 8 66-67). However, Gatherer et al. does not explicitly discloses having serial packet sync encoder comprises a serial packet sync transmitter that transmits said serial packet sync datastream on a single pin. Krieger disclose having a encoder 116 at the transmitter is a SCTCM encoder (serially concatenated trellis coded modulation, column 5 line 41-42).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a encoder 28 as taught by Gatherer et al. that is a SCTCM encoder (serially concatenated trellis coded modulation, column 5 line 41- 42) that comprises a transmitter as taught by Krieger to provide a technique that will encode each bit in order to detect errors within the data words that are transmitted .

18. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mannett et al. (US Patent 6,975,652) in view of Bobeck et al. (US patent 6,075,787).

With regard to claim 20, Mannett et al. discloses a *system for receiving indication of an event,* Mannett et al. discloses having a HFC network 124 that be a two-way, cable TV-capable network that utilize broadcast downstream transmission and a combination of FDM/TDM for upstream transmission to privde voice and data services (column4 line 16-19).

a serial packet sync receiver that receives a serial packet sync datastream on a single

pin, Mannette et al. disclose having CM (cable modem) that is responsible for receiving control messages from the CMTS and taking appropriate action based on these messages (column 9 line 45-50). Mannette et al. further discloses a CMTS transmit information to a receiving device 500 ("serial packet receiver") receiving a MAC syn message (column 10 line 1-20). However, Mannette does not explicitly discloses receiving packet sync datastream on a single pin. Bobeck et al. discloses having a cable modem receivers ("serial packet syn receiver") whereby the receiver identifies each occurrence of the bit patterns '1010xyzw' and then identifies the bit patterns after 479 bytes to check that the super frame counter 530 has incremented by one (column 10 line 46-65). It is inferred the bit patterns are being process through a superframe counter 530 in a single instance .

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a CM (cable modem) that is responsible for receiving control messages from the CMTS as taught by Mannette et al. receiving bit patterns and being process by a super frame counter 530 in one instance as taught by Bobeck et al. whereby reducing the cost of the cable modem.

a preamble comparator that compares said received serial packet sync datastream to determine if said received serial packet sync datastream matches a preamble and a holding register for holding a packet sync vector included in said serial packet sync datastream. Mannette et al. discloses having the MPEG frame recover block 514 is

coupled to MAC sync message detector 516. The MAC sync message detector 516 has a strobe ("preamble comparator"), which coupled to timestamp registers 520, 522, 524, and 526 ("holding registers"), and the MAC sync message detector remote timestamp is coupled to registers 520. The registers 520 and 522 are coupled to modulo compare block 528 and register 520 coupled to register 522... (column 10 line 12-29)... timestamp registers 520,522,524, and 526 stores numerical values, which are representative of time. The values in these registers are latched by the strobe that comes from the MAC synchronous message detector 516...the modulo compare block 528 and 530 compares two different inputs and make a determination concerning the difference between the two inputs. The modulo compare block 530 determines the period of the local (CM) clock while the modulo compare block 528 determines the period of the remote clock (column 11 line 15-37). It is inferred that the MAC sync message is evaluated by the MAC message detector 516 and put into timestamp registers ("holding registers") they are compared to the information that is given by the CMTS.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DeWanda Samuel whose telephone number is (571) 270-1213. The examiner can normally be reached on Monday- Thursday 8:30-5:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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DeWanda Samuel
12/3/2007

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